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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/045,376	11/09/2001	Brian S. Doyle	42390.P5768D	5627		
8791	7590 09/24/2002					
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025			EXAM	EXAMINER		
			LE, DUNG ANH			
			ART UNIT	PAPER NUMBER		
			DATE MAILED: 09/24/2002	DATE MAILED: 09/24/2002		

Please find below and/or attached an Office communication concerning this application or proceeding.

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•	Offic	Action Summary	Exami	ner	Art Unit	
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1)	Responsi	ive to communication(s) fi	iled on 00 Novembe	r 2001		
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•	on of Clair					
		1-18 is/are pending in the				
		above claim(s) is/a	re withdrawn from o	consideration.		
		is/are allowed.				
		<u>-9 and 13-18</u> is/are reject	ed.			
		0-12 is/are objected to.				
	on Papers	are subject to restric	ction and/or election	requirement.		
9)[] 7	he specific	cation is objected to by the	e Examiner.			
10) <u> </u>	he drawing	g(s) filed on is/are:	a) accepted or b)	objected to by the Exam	iner.	
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40\C\ T		d, corrected drawings are red		Office action.		
		declaration is objected to	by the Examiner.			
		S.C. §§ 119 and 120				•
		gment is made of a claim	for foreign priority u	inder 35 U.S.C. § 119(a)-	(d) or (f).	
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)  Notice )  Informa	of Draftspersonation Disclosu	s Cited (PTO-892) on's Patent Drawing Review (PT re Statement(s) (PTO-1449) Pa		4) Interview Summary (F 5) Notice of Informal Pat 6) Other:	PTO-413) Paper No(sitent Application (PTO	) -152)
Patent and Trac O-326 (Rev.			Offic Acti n Summa		Part of	Paper No. 2

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#### **DETAILED ACTION**

#### Oath/Declaration

The oath/declaration filed on 11/09/2001 is acceptable.

### Specification

The specification is objected to for the following reason:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP § 606.01).

A new abstract is required that is clearly indicative the invention to which the claims are directed. Note that, the claims are directed to semiconductor device instead of to a method of making a semiconductor device.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## Claim Rejections

## Set of claims 1-7

# Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless --

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2 and 5-7 are rejected under 35 USC 102 (e) as being anticipated by Kokubun (6248652).

Kokubun disclose an apparatus comprising:

a substrate having a source region 6, a drain region 6, and a channel region having a void 4 (col 1, lines 55- 57 and lines 60- 67) and to provide a barrier to lines of force to reduce leakage current (Figs.7(a)-7(c).

**Regarding claim 2**, void is located substantially in a center of said channel region (Fig. 7(b)).

Regarding claim 5, a gate region (Fig. (c)).

Regarding claim 6, void 4 is located near an edge of channel region adjacent to source region 6 (Fig. (c)).

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Regarding claim 7, a void 4 located near an edge of the channel region adjacent drain region 6 (Fig. (c)).

#### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kokubun (6248652) as applied to claim 1 above, and further in view of the remark.

Kokubun teach, in figures 7(a)-7(c), void is a undisclosed across in channel region, but fails to teach void is approximately 50 nm across.

It would have been obvious to one having ordinary skill in the art making semiconductor device to determine the workable or optimal value for void is approximately 50 nm across through routine experimentation and optimization to optimal device performance.

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Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kokubun (6248652) as applied to claim 1 above, and further in view of Akatsu et al. (6329271).

Kokubun teach, in figures 7(a)-7(c), void is located at a undisclosed depth in gate region, but fails to teach void is located at a depth of approximately 1000 angstroms in gate region.

However, Akatsu et al. show a void 16 (figs. 3-6). It is typically is 30-50 nm (300 - 500 Angstroms) below the surface 10A. (col 4, lines 17-23)

It would have been obvious to one having ordinary skill in the art making semiconductor device to determine the workable or optimal value for void is located at a depth of approximately 1000 angstroms in gate region through routine experimentation and optimization to optimal device performance.

## Set of claims 8-14

Claims 8, 9 and 13 are rejected under 35 USC 102 (e) as being anticipated by Kokubun (6248652).

Kokubun disclose an apparatus comprising:

a gate region 5; and a substrate having a source region 6, a drain region 6, a channel region, and a void 4 below source region 6 to provide a barrier to lines of force to reduce leakage current (figs. 7(a)-(c).

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Regarding claim 9, a void is located below drain region 6 (figs. 7(a)-(c).

Regarding claim 13, gate region 8 is polysilicon (col 8, line 38).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kokubun (6248652) as applied to claim 8 above, and further in view of Adan (6288425).

Kokubun discloses gate region is conductive material (e.g. polysilicon in column 4, line 38), but fails to disclose gate region is metal.

However, Adan show the gate region is make of polysilicon, metal as set forth in column 4, lines 18-22. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate region of metal as taught by Adan in Kokubun's device because the material such as polysilicon and metal are recognized equivalent materials for forming the gate region of transistor and they are interchangeable.

Claims 10, 11 and 12 are objected (refer to Allowable Subject Matter below)

**Set of claims 15-18.** 

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Claims 15 and 17 are rejected under 35 USC 102 (e) as being anticipated by Kokubun (6248652).

Kokubun discloses an apparatus comprising a gate region having a void 4 to provide a barrier to lines of force to reduce leakage current; and

a substrate 1 having a source region 6, a drain region 6, and a channel region (figures 7(a)-7(c).

Regarding claim 17, gate region is polysilicon (col 8, line 38).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kokubun (6248652) as applied to claim 15 above, and further in view of Akatsu et al. (6329271).

Kokubun teach, in figures 7(a)-7(c), void is located at a undisclosed depth in gate region, but fails to teach void is located at a depth of approximately 1000 angstroms in gate region.

However, Akatsu et al. show a void 16 (figs. 3-6). It is typically is 30-50 nm (300 - 500 Angstroms) below the surface 10A. (col 4, lines 17-23)

It would have been obvious to one having ordinary skill in the art making semiconductor device to determine the workable or optimal value for void is located at a depth of approximately 1000 angstroms in gate region through routine experimentation and optimization to optimal device performance.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kokubun (6248652) as applied to claim 15 above, and further in view of Adan (6288425).

Kokubun discloses gate region is conductive material (e.g. polysilicon in column 4, line 38), but fails to disclose gate region is metal.

However, Adan show the gate region is make of polysilicon, metal as set forth in column 4, lines 18-22. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate region of metal as taught by Adan in Kokubun's device because the material such as polysilicon and metal are recognized equivalent materials for forming the gate region of transistor and they are interchangeable.

#### Allowable Subject Matter

Claims 10, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Adan (U.S. Patent No. 6288425) and Kokubun (U.S. Patent No. 6248652), taken individually or in combination, do not teach the claimed invention having source region and said drain region are under compressive stress (Regarding

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claim 10); source region is under tensile stress (Regarding claim 11), and drain region is

under compressive stress 9 (Regarding claim 12).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is 703-306-5797. The examiner can normally be reached on Monday-Friday 8:00am-5: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Dung A. Le X

Dung A. Le

Examiner

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